HBCU CHIPS NETWORK

ANNUAL CONFERENCE

APRIL 3-4, 2025

PROGRAM BOOK

The Armour J. Blackburn University Center
2397 Sixth Street NW
Washington, DC 20009

Advancing Semiconductor Leadership Through HBCU Innovation

Build boldly.
Innovate fearlessly.

At Micron, we don't just imagine the future — we build it. We are accelerating intelligence in AI through groundbreaking, industry-leading technology to enable smarter, more responsive applications that transform industries and enhance everyday life.

The HBCU CHIPS Network is fueling the next generation of leaders in microelectronics, ensuring that opportunities to innovate reach every community. We are committed to this vision, as we plan to invest more than $140 billion in leading-edge memory manufacturing and R&D in the United States. We need your passion, your ideas, and your drive to power the breakthroughs that will transform how the world uses information to enrich life *for all*. If you're ready to push boundaries, challenge expectations and create what's next, your future starts here.

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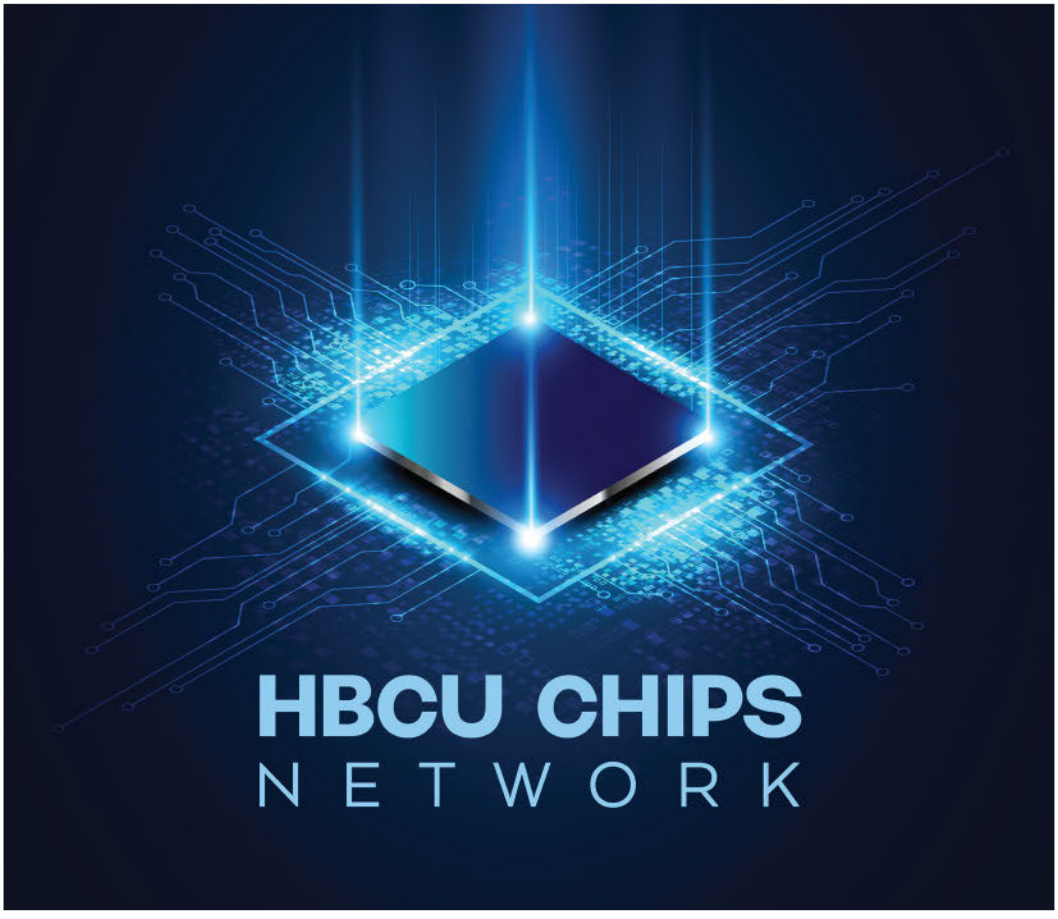

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Advancing Semiconductor Leadership Through HBCU Innovation

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Dear Esteemed Guests, Participants, and Colleagues,

Welcome to the **HBCU CHIPS Network Conference!** We are delighted to have you join us for this pivotal gathering, where we celebrate and advance the role of Historically Black Colleges and Universities (HBCUs) in shaping the future of semiconductor research and innovation.

This conference serves as a dynamic platform for collaboration, knowledge exchange, and networking among students, faculty, industry professionals, and policymakers. We are honored to bring together a diverse community of thought leaders and innovators dedicated to strengthening the semiconductor and microelectronics ecosystem within our institutions and beyond.

Over the next few days, you will engage in insightful discussions, attend thought-provoking sessions, and participate in hands-on workshops designed to equip you with the skills and knowledge needed to thrive in the ever-evolving semiconductor industry. We encourage you to take full advantage of this unique opportunity to connect with peers, share your experiences, and foster meaningful collaborations.

We extend our deepest gratitude to our sponsors, partners, and volunteers, whose unwavering support has made this conference possible. Your commitment to fostering opportunities for HBCUs in semiconductor research and microelectronics is truly invaluable.

As we embark on this journey together, let us challenge ourselves to innovate, collaborate, and empower the next generation of leaders in semiconductor research.

Thank you for being here. We look forward to an inspiring and productive conference!

Warm regards,

The HBCU CHIPS Network Conference Committee

HBCU CHIPS Network Mission

The mission of the HBCU CHIPS Network is to cultivate a diverse and skilled workforce to support the U.S. semiconductor industry.

This mission directly addresses the CHIPS for America program's requirement for addressing the "Missing Millions" problem by fostering opportunities for disadvantaged communities. The network can achieve this by:

- *Advancing U.S. leadership in microelectronics technology*: Leveraging the collective research expertise, capabilities, infrastructure, and core competencies of HBCUs.
- *Developing and implementing innovative educational programs*: This will involve creating a specialized curriculum in semiconductor design, fabrication, and related fields, along with internship and research opportunities in collaboration with industry partners.
- *Facilitate collaboration and knowledge sharing*: Bringing together researchers from various HBCUs to encourage interdisciplinary research and innovation in areas critical to microelectronics development.
- *Providing scholarships and financial aid*: Making higher education in these fields accessible to underrepresented students from HBCUs is crucial to increasing diversity in the workforce.
- *Promoting outreach and mentorship programs*: Connecting students with industry professionals and successful individuals from HBCUs to inspire and guide them in pursuing careers in the semiconductor industry.
- *Secure funding and resources*: The network will act as a unified voice for HBCUs to advocate for funding opportunities and partnerships with government agencies and private companies involved in the CHIPS and Science Act initiatives.
- *Foster innovation and entrepreneurship*: The Network will support HBCU students and faculty in developing and commercializing their research findings, potentially leading to groundbreaking advancements in the semiconductor field.

By fulfilling its mission and achieving its vision, the HBCU CHIPS Network can play a pivotal role in ensuring the success of the CHIPS and Science Act while promoting diversity, equity, and inclusion in the U.S. semiconductor industry.

HBCU CHIPS Network Vision

The HBCU CHIPS Network is envisioned as a research and education consortium that serves as the nexus of collaboration and cooperation between HBCUs, government agencies, academia, and industry. Through our collaborative efforts the Network will play a defining role in helping the U.S.A. regain leadership in microelectronics while addressing the global challenges that currently plagued this industry. Through a multidisciplinary approach the Network will facilitate fulfilling talent pipelines to grow the workforce of the future, research innovations, resolving long standing disparities in facilities, building out domestic capacity and providing shared accessibility across the Network stakeholders. Additionally, the Network will provide outreach to community colleges, veterans, and K-12, thus empowering a diverse, and inclusive workforce that leverages research innovations including experiential learning opportunities across all stakeholder groups. If the US is serious about reshoring this critical industry, then to quote the Honorable Secretary of Commerce Gina Raimondo at the official HBCU CHIPS Networking Kick-Off meeting in Washington, DC at the Department of Commerce, "We must have all hands on-deck if the U.S. is to be successful in its reshoring efforts." This plan outlines the creation of an independent consortium consisting of representatives from the HBCUs and other stakeholder groups to serve as the convening and governing body for the Network that makes key decisions and recommendations that support and grow minority participation in microelectronics.

About The HBCU CHIPS Network Conference

The **HBCU CHIPS Network Inaugural Conference** will convene leading scholars, industry experts, government officials, faculty and students from **Historically Black Colleges and Universities (HBCUs)** to discuss advancements, and opportunities in **semiconductor research and microelectronics**. The conference will serve as a platform for fostering collaboration, strengthening research capabilities, and positioning HBCUs as key players in the national semiconductor ecosystem. Through plenary sessions, panel discussions, keynote presentations, workshops and technical sessions, attendees will engage with thought leaders in semiconductor research and microelectronics. The conference will lay the foundation for strengthening HBCU contributions to semiconductor research and workforce development, while fostering collaborations, showcasing cutting-edge research, and positioning HBCUs as vital partners in **advancing U.S. semiconductor leadership**. The conference will also set the stage for ongoing initiatives, including funding opportunities, industry partnerships, and student training programs in microelectronics.

HBCU CHIPS NETWORK MEMBER INSTITUTIONS

- Alabama A&M University
- Alabama State University
- Bowie State University
- Central State University
- Clark Atlanta University
- Delaware State University
- Dillard University
- Florida A&M University
- Fort Valley State University
- Georgia Institute of Technology
- Hampton University
- Howard University
- J.F. Drake State Community & Technical College
- Jackson State University
- Meharry Medical College
- Morehouse College
- Morgan State University
- Norfolk State University
- North Carolina A&T State University
- Prairie View A&M University
- Savannah State University
- Southern University and A&M College
- Spelman College
- Tennessee State University
- Texas Southern University
- Trenholm State Community College
- Tuskegee University
- University of the District of Columbia
- Virginia State University
- Wilberforce University
- Winston Salem State University

HOWARD UNIVERSITY

Office of Research

A CARNEGIE RESEARCH ONE (R-1) UNIVERSITY

- FIRST HBCU LED DEPARTMENT OF DEFENSE, UNIVERSITY AFFILIATED RESEARCH CENTER (RESEARCH INSTITUTE FOR TACTICAL AUTONOMY)
- TOP PRODUCER OF AFRICAN AMERICAN UNDERGRADUATES WHO LATER EARN DOCTORAL DEGREES IN STEM
- HIGHEST NUMBER OF HBCU RHODES SCHOLARS & MARSHAL SCHOLARS
- TOP 100 ON U.S. NEWS & WORLD REPORT BEST COLLEGES
- 120 UNDERGRADUATE PROGRAMS, 50 MASTERS AND DOCTORAL DEGREE PROGRAMS, 5 PROFESSIONAL PROGRAMS
- PROFESSIONAL DEGREES PROGRAMS : MEDICINE (M.D.), LAW (J.D.), DENTISTRY (D.D.S.) , PHARMACY (PHARM.D.)
- STEM UNDERGRADUATE DEGREE PROGRAMS:
  - BIOLOGY
  - CHEMICAL ENGINEERING
  - CHEMISTRY
  - CIVIL ENGINEERIING
  - COMPUTER SCIENCE
  - COMPUTER INFORMATION SYSTEMS
  - ELECTRICAL ENGINEERING
  - MATHEMATICS
  - MECHANICAL ENGINEERING
  - PHYSICS
- STEM DOCTORAL DEGREE PROGRAMS:
  - ATMOSPHERIC SCIENCES
  - BIOLOGY
  - BIOMEDICAL & CHEMICAL ENGINEERING
  - BIOMEDICAL SCIENCES
  - CHEMICAL ENGINEERING
  - CHEMISTRY
  - CIVIL & ENVIRONMENTAL ENGINEERING
  - COMPUTER SCIENCE
  - ELECTRICAL ENGINEERING
  - MATHEMATICS
  - MECHANICAL ENGINEERING
  - PHYSICS

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Google

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Google is proud to partner with the HBCU CHIPS Network Conference to expand opportunity for communities everywhere.

Expanding Opportunities.

Elevating Leaders.

SRC and SMART USA are proud to empower HBCU talent to lead the American chip revolution.

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SMART USA

Training All People

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- Superior Skill Development
- Each Trainee Gets Their Own Factory
- Exact Experience That Employers Want

HBCU CHIPS NETWORK AGENDA

Thursday, April 3

7:00 AM - 8:30AM **Event Registration and Breakfast**

Location: The Ballroom

8:30 AM - 8:50AM **Welcome and Opening remarks**
Pamela A.G, Clarke, Sr.
Director of Research Development
Howard University

Bruce Jones, Ph.D., Sr.
Vice President for Research
Howard University

Anthony K. Wutoh, Ph.D.
Provost & Chief Academic Officer
Howard University

Ben Vinson III, Ph.D.
President, Howard University

Location: The Ballroom

8:50 AM - 9:00 AM **Keynote Speaker Introduction**
George White, Ph.D.
Director Strategic Partnerships
Georgia Institute of Technology

Location: The Ballroom

9:00 AM - 9:50 AM **Keynote Address**
Thomas Caulfield, Ph.D.
President, and CEO Global Foundries

Location: The Ballroom

10:00 AM -10:20 AM **Apple New Silicon Initiative**
Ramesh Abhari, PhD
Michael A. Smith, PhD*
Jared Zerbe
** Presenter*
Location: The Ballroom

10:20 AM -10:30 AM **Coffee Break**

Location: The Ballroom

10:30 AM - 11:30 AM **Panel: Academic-Industry Partnerships in Semiconductor Research &Development**

MODERATOR: Donnell Walton, Ph.D.
Deputy Director, RITA UARC

PANELISTS: Danielle Ferguson-Macklin
Global DEI Program Manager, Teradyne

Michelle Williams
Executive Director, Semi Foundation

Denise Evans
Manager Systems Engineer, Northrop -Grumman Mission Systems Division

Jeremy Muldavin, Ph.D.
Director, Sales Development A 7D, Cadence

Location: The Ballroom

11:30 AM – 12:30 PM **Panel: Role of Artificial Intelligence (AI) in Semiconductor Development: How AI is Revolutionizing CHIP Design and Verification**

MODERATOR: Sonya Smith, Ph.D.
Professor & Executive Director, RITA UARC

PANELISTS: Ron Duncan
Head of Innovation Programs
Chief Innovation Office, Synopsys

Hassan Salmani, Ph.D.
Associate Professor, Electrical Engineering & Computer Science, Howard University

Dinadayalane Tandbany, Ph.D.
Professor, Chemistry
Clark Atlanta University

William Chapman, Ph.D.
Postdoctoral Research Fellow
Sandia National Laboratories

Location: The Ballroom

12:30 PM – 2:00 PM **Lunch**

Student Achievement in Microelectronics Awards Ceremony

HBCU CHIPS Network Conference Committee

Micron Education Hub Presentation
Ariela Gruszka
TPG University Project Manager, Micron

Location: The Ballroom

2:00 PM - 3:00 PM **Tabling & Networking**

Location: The First & Second Floor Lobby

3:00 PM - 4:30 PM

Breakout Room 1: Technology& Design

SESSION CHAIRS: Dinadayalane Tandabany
Clark Atlanta University

Kevin Kornegay
Morgan State University

Oral Research Presentations:

Eniola Ajegbemikka
North Carolina A & T State University

Malcolm Bogroff
Howard University

Mahdi Hasanzadeh
North Carolina A & T University

Theodore Johnson
Intel

Kevin Kornegay
Morgan State University

Location: The Reading Lounge

Breakout Room 2: Materials & Fabrication

SESSION CHAIRS: Vanessa Smet
Georgia Institute of Technology

Eric Seabron
Howard University

Oral Research Presentations:

Joshua Burrow
Morgan State University

Baraka Chimba
Alabama A &M University

Sugata Chowdhury
Howard University

Ningxin Li
Clark Atlanta Universit y

Monté Hendrix
Morgan State University

Zhiping Luo
Fayetteville State University

Indika Senevirathna
Clark Atlanta University

Michael Spencer
Morgan State University

Location: The Gallery Lounge

Breakout Room 3: Quantum & Photonics

SESSION CHAIRS: Shyam Aravamudhan
North Carolina A&T State University

Demetris Geddis
Hampton University

Oral Research Presentations:

Jose Azucena
North Carolina A&T State University

Robert Coleman
Howard University

Vineet Kumar Sharma
Howard University

Cameron Lewis
Howard University

Sheikh Mahtab
Morgan State University

Daniel Vrinceanu
Texas Southern University

Indika Senevirathna
Clark Atlanta University

Michael Spencer
Morgan State University

Location: The Digital Auditorium

Breakout Room 4 : Applications & Sustainability (Industry Tutorials)

SESSION CHAIRS: Hassan Salmani
Howard University

Oral Research Presentations:

David Lockett
Meharry Medical College

Michelle Williams
SEMI Foundation

Industry Presentations:

Ron Duncan
Head of Innovation Programs
Chief Innovation Office, Synopsys

Location: The Forum

4:30 PM - 4:45 PM

Announcements

The HBCU CHIPS Network Initiating Committee

Location: The Ballroom

4: 45 PM – 5:00 PM **TAPE-OUT Discussion – Global Foundries**
"Invitation Only"
Location: The Reading Lounge

5:00 PM - 7:00 PM **Reception**
Location: The Ballroom

Friday, April 4

7:00 AM – 8:00AM **Event Registration and Breakfast**
Location: The Ballroom

8:00 AM –8:15 AM **Welcome and Introduction of CEO Fireside Chat Speaker & Moderator**
George White, Ph.D.
Director Strategic Partnerships
Georgia Institute of Technology
Location: The Ballroom

8:15 AM – 9:00 AM **CEO Fireside Chat**
MODERATOR: Erin Lynch, Ph.D.
President, Quality Education for Minorities (QEM) Network
SPEAKER: Todd Younkin, Ph.D.
CEO and President
Semiconductor Research Corporation
Location: The Ballroom

9:00 AM - 10:00 AM **Panel: Workforce Development for the Semiconductor Industry**
MODERATOR: Talitha Washington, Ph.D.
Center for Applied Data Science & Analytics
PANELISTS: Brian Best
IT Director, Micron
Carl McCants, Ph.D.
Special Assistant to the DARPA Director, Defense Advanced Research Projects Agency
Patricia Mead, Ph.D.
Professor & Department Chair
Norfolk State University
Location: The Ballroom

10:00 AM – 10:30 AM **Break: Tabling & Networking**
Location: The First & Second Floor Lobby

10:30 AM - 11:30 AM **Panel: The Future of Semiconductor Design and Manufacturing**
MODERATOR: Kevin Kornegay, Ph.D.
Deputy Director, Eugene Deloatch Endowed Professor, Morgan State University
PANELISTS: Ron Duncan
Head of Innovation Programs
Chief Innovation Office, Synopsys
Greg Pickrell, Ph.D.
Domain Chief Engineer – Microfabrication, Sandia National Laboratories
Antonio de la Serma
Principal Director
Strategic Technologies, Siemens EDA
Robert Sarkkissian
Director Aerospace and Defense Sector
Cadence Design Systems
Location: The Ballroom

11:30 AM –1:00 PM **Lunch**

CollabNext Presentation
Lew Lofton, Ph.D.
Georgia Institute of Technology
Firdous Kausar
Fisk University
Beverly Robinson
Fisk University
Hina Raja
Fisk University
Location: The Ballroom

1:00 PM - 2:00 PM **Tabling & Networking**
Location: The First & Second Floor Lobby

2:00 PM -3:45PM **Breakout Room 1: Technology& Design**
SESSION CHAIRS: Daniel Vrinceanu
Texas Southern University
Shyam Aravamudhan
North Carolina A&T State University

Oral Research Presentations:
Shyam Aravamudhan
North Carolina A&T State University
Xuemin Chen
Texas Southern University
Kishak Cinfawtm
Morgan State University

Mehdi Elahi
North Carolina A & T State University

Mahsa Tahghigh
Howard University

Anu Upadhyaya
Howard University

Location: The Reading Lounge

Breakout Room 2: Materials & Fabrication

SESSION CHAIRS: Patricia Mead
Norfolk State University
Frances Williams, Clark Atlanta University

Oral Research Presentations:
Ashwaq Bahkali
Texas Southern University

Daemar Casey
Delaware State University

Anirban Goswami
Howard University

Kristen Harris
Alabama A &M University

Daniel Harrison
Morgan State University

Malachi Moody
Delaware State University

Miles Phifer
North Carolina A&T State University

Location: The Gallery Lounge

Breakout Room 3: Quantum & Photonics

SESSION CHAIRS: Darwish Abdalla
Dillard University

Mohammadreza Hadizadeh
Central State University

Oral Research Presentations:
Darwish Abdalla
Dillard University

Ashutosh
Howard University

Mohammadreza Hadizadeh
Central State University

Muubbashar Khan
Central State University

Joao Prioli
North Carolina A&T University

Eric Seabron
Howard University

Location: The Digital Auditorium

Breakout Room 4: Applications & Sustainability (Industry Tutorials)

SESSION CHAIRS: Michael Curry
North Carolina A&T State University

Niya King
North Carolina A&T State University

Oral Research Presentations:
Suxia Cui
Prairie View A&M University

Kinnis Gosha
Morehouse College

Thong Le
Norfolk State University

Industry Presentations:
Joanna Pritchard, Ph.D.
Global Academic Strategy & Engagement, Siemens

Location: The Forum

Breakout Room 5: Micron DRAM Array Virtual Reality Experience
"Invitation Only"

Location: Truth & Service

3:45 PM - 4:00 PM **Closeout Session**
The HBCU CHIPS Network Initiating Committee

Location: The Ballroom

SPEAKER AND PANELIST BIOGRAPHIES

Keynote Speaker

Name: Thomas Caulfield, Ph.D.
Title: Executive Chairman of the Board for GlobalFoundries
Organization: Global Foundries
Bio: Dr. Thomas Caulfield is the President and CEO of GlobalFoundries, leading the company since March 2018 and overseeing its landmark IPO in October 2021. He joined GlobalFoundries in 2014 as Senior Vice President and General Manager of Fab 8. With a rich career in engineering and executive management, Dr. Caulfield has held key roles at Soraa, Ausra, Novellus Systems, and IBM. He also serves on the board of Western Digital Corporation. Dr. Caulfield holds a Bachelor of Science in Physics from St. Lawrence University and advanced degrees in Materials Science and Engineering from Columbia University.

CEO Fireside Chat Speaker

Name: Todd Youngkin
Title: CEO, Semiconductor Research Corporation
Organization: Semiconductor Research Corporation (SRC)
Bio: Dr. Todd Younkin is the CEO of the Semiconductor Research Corporation (SRC) and Executive Director of the newly awarded SMART USA Digital Twin Manufacturing Institute. He is responsible for >$100M annually in sponsored research and education that involves over 100 universities, 25 companies, and 3 U.S. government agencies. Todd oversaw the release of the 2030 Decadal Plan for Semiconductors, which bolstered the case for passage of the 2022 CHIPS and SCIENCE ACT, followed by the 2023 release of the Microelectronics and Advanced Packaging Technologies (MAPT) Roadmap, which provided guidance on how to tackle the technical challenges outlined in the Decadal Plan. Todd now serves on the Secretary of Commerce's Industrial Advisory Committee (IAC) in support of CHIPS for America. Prior to leading SRC, Dr. Younkin worked at Intel from 2001-2020, with research and development experience spanning Intel's 0.18um to 5nm nodes in a variety of business units. He has a B.S. in Chemistry from the University of Florida and a Ph.D. in Organometallic and Polymer Chemistry from the California Institute of Technology. In his free time, Todd enjoys skiing, playing tennis, and walks with his Golden Retriever.

Moderators and Panelists *(Alphabetical Order)*

Name: Brian Best
Title: IT Director
Organization: Micron
Bio: Brian is the IT Director at Micron in Manassas, VA. With over 40 years of experience in the industry, he has a wealth of knowledge and expertise. Brian holds a BS in Computer Science, with minors in Black Studies and Business Administration. Following his time in the US Air Force, he joined IBM as a Software Engineer, where he was recognized for many key accomplishments and contributions to the company's success. In 2002, Brian joined Micron, where he's now accountable for all IT operations at our Manassas facility. His role involves ensuring the smooth functioning of IT systems, supporting his teams, and contributing to Micron's global IT strategy.

Name: William Chapman
Title: Postdoctoral Research Fellow
Organization: Sandia National Laboratory
Bio: William is a postdoctoral fellow in neuromorphic computing at Sandia National Laboratories. His research focuses on biologically inspired machine learning algorithms for processing temporal data, self-supervised local learning, edge processing, and codesign of algorithms with neuromorphic circuits. He holds a PhD in computational neuroscience from Boston University.

Name: Antonio de la Serna
Title: Principal Director, Strategic Technologies, Siemens EDA
Organization: Siemens
Bio: A 40-year career in start-ups, research labs, large corporations, and government. I have served as - Advisory board member at U.S. engineering universities, Former Vice Chair, Regional Workforce Investment Board, Massachusetts, Former National Vice President, MAES: Latinos in Science & Engineering and Senior Member, IEEE.

Name: Ron Duncan
Title: Head of Innovation Programs, Chief Innovation Office
Organization: Synopsys
Bio: "Ron has leadership experience in various semiconductor-related areas from TCAD to physical implementation. He currently focuses on emerging technology applications such as AI, quantum/ superconducting computing, automotive electronics, neuromorphic computing, and silicon photonics. He represents Synopsys at a variety

of international conferences and government research symposiums. Ron received Electrical Engineering degrees from MIT and Cornell University. Prior to Synopsys, he held management and technical positions at Avant!, ISS and Hewlett Packard. He is a Synopsys Excellence Award Winner and co-leads the Synopsys Black Employee Resource Group (ERG), "VIBE."

Name: Denise Evans
Title: Manager Systems Engineer
Organization: Northrop Grumman
Bio: Denise is a graduate of Morgan State University with a bachelor's degree in electrical and computer engineering. She is currently a member of the Northrop Grumman family fulfilling her role as a Manager Systems Engineer where she provides guidance on career development for 20 physicists. Denise is also the Microelectronics Academy Deputy Lead, the technical lead for more than 50 engineers, physicists, and technicians. For the majority of her career, Denise has supported the DoD serving as both, contractor and government civilian, where she utilized her technical and leadership subject matter expertise to the successful completion of various programs .

Name: Danielle Ferguson-Macklin
Title: Global DEI Program Manager
Organization: Teradyne
Bio: As a dynamic and innovative leader, I have eight years of experience spearheading Diversity, Equity, and Inclusion (DE&I) programs and initiatives and over twenty years of experience managing change and developing talent at the largest U.S. cable internet access provider. My areas of expertise include business analytics, inclusive leadership, change management, and an understanding of human history and culture.

While at Teradyne, I have created partnerships and programs that have contributed to organizational success in fostering company culture, happiness, and connection. We are committed to making Teradyne a global organization that reflects the multiplicity of the world we live in. As a proud Big Sister to a rising senior at Old Dominion University, I believe in the power of authentic, compassionate, and honest coaching and mentoring that adds value to our next generation of global leaders. I joined Teradyne in 2021 as a DEI Program Manager to help foster a collaborative culture that will create a stronger and more resilient company for our employees, customers, and communities. I hold a BS in Business Administration from Southern New Hampshire University and a Master of Public Administration from Rutgers University.

Name: Kevin Kornegay
Title: Eugene DeLoatch Endowed Professor
Organization: Morgan State University
Bio: Kevin T. Kornegay received a B.S. degree in electrical engineering from Pratt Institute, Brooklyn, NY, in 1985 and an M.S. and Ph.D. in electrical engineering from the University of California at Berkeley in 1990 and 1992, respectively. He is the Eugene DeLoatch Endowed Professor and Director of the Cybersecurity Assurance and Policy (CAP) Center at Morgan State University in Baltimore, MD. His research interests include hardware assurance, hardware/software reverse engineering, system-on-chip (SoC) design, secure embedded systems, and secure autonomy. He serves on the technical program committees of several international conferences, including the IEEE Symposium on Hardware Oriented Security and Trust (HOST), the IEEE Secure Development Conference (SECDEV), USENIX Security 2020, the IEEE Physical Assurance and Inspection of Electronics (PAINE), the IEEE Symposium on VLSI Technology and Circuits, and the ACM Great Lakes Symposium on VLSI (GLSVLSI). He serves on the NIST IoT Advisory Board, the State of Maryland Cybersecurity Council, and the NIST Industrial Advisory Council R&D Workforce Working Group. He has received numerous awards, including the NSF CAREER Award, IBM Faculty Partnership Award, National Semiconductor Faculty Development Award, and the General Motors Faculty Fellowship Award. He is an AAAS Fellow, a Life Member of the IEEE, and a member of the Eta Kappa Nu, Sigma Xi, and Tau Beta Pi engineering or scientific research honor societies.

Name: Carl McCants
Title: Special Assistant to the Director, DARPA
Organization: Defense Advanced Research Projects Agency (DARPA)
Bio: Dr. Carl E. McCants is a special assistant to the DARPA director, focusing on efforts to inform microelectronics policy and national strategies for microelectronics R&D. Before this, he was the technical director of the Supply Chain and Cyber Directorate at NCSC, senior program manager at IARPA, program manager at DARPA MTO, chief technologist to the MTO office director, special assistant to the DARPA deputy director, and a project manager at Agilent Technologies. He received his bachelor's degree from Duke University in 1981 and master's and doctoral degrees from Stanford University in 1982 and 1989, respectively, all in EE.

Name: Jeremy Muldavin
Title: Director Sales Development A&D
Organization : Cadence
Bio: Dr. Jeremy Muldavin is a Director Sales Development at Cadence. He brings an exceptional background in electrical engineering, holding a Ph.D. from the University of Michigan, and over two decades of leadership in cutting-edge microelectronics, advanced technology systems, and defense applications. His career spans pivotal roles in government, academia, and industry, including MIT Lincoln Laboratory, GlobalFoundries, and the Office of the Undersecretary of Defense for Research and Engineering. Jeremy is renowned for his expertise in semiconductor traceability, microelectronics assurance, and advanced RF systems, and he has contributed significantly to national security initiatives. Beyond his technical acumen, Jeremy is an advocate for STEM outreach and collaboration.

Name: Greg Pickrell
Title: Domain Chief Engineer – Fabrication
Organization: Sandia National Laboratory
Bio: Greg Pickrell, Ph.D., is the Domain Chief Engineer for Fabrication at Sandia's Microsystems Engineering, Science and Applications (MESA) center. With over 25 years of experience in the private sector and at Sandia, he has led research, maturation, and production of semiconductor devices, including power electronics, lasers, and photodetectors. He has also led heterogeneous device integration for Silicon Photonics. Greg has directed multiple Product Realization Teams and served as Principal Investigator on various R&D projects. He earned his Ph.D. from the University of Illinois at Urbana-Champaign in 2002 and is a Senior Member of IEEE.

Name: Hassan Salmani
Title: Associate Professor
Organization : Howard University
Bio: Hassan Salmani is an Associate Professor within the Department of Electrical Engineering and Computer Science at Howard University. His research endeavors revolve around hardware security and trust, Internet of Things security and the development of reliable systems. He is the author of two books: "Integrated Circuit Authentication: Hardware Trojans and Counterfeit Detection" and "Trusted Digital Circuits – Hardware Trojan Vulnerabilities, Prevention, and Detection." Additionally, he has contributed a number of papers to the field of hardware assurance design. His research is generously supported by organizations including NASA, the Air Force, Navy, Army, DARPA, Lockheed Martin, and the Department of Education.

Name: Robert Sarkissian
Title: Director Aerospace and Defense Sector, Cadence Design Systems
Organization: Cadence
Bio: Mr. Robert Sarkissian holds a BS in Physics from Florida Tech. His career spans some 40 years in both the Electronic Design Automation Industry and Systems Engineering. He has devised and provided engineering solutions based on MBSE principles for Boeing Commercial Airplanes and their Defense Business, Lockheed Martin, Northrop Grumman, BAE Systems, L3Harris, Raytheon, the Air Force, ARMY, and NAVY, DARPA, and others. He has also championed many University Programs associated to both R&D and Workforce Development. He currently is leading his company's efforts in the heavily promoted CHIPS and SCIENCES ACT (2022) and is seeking the introduction of the convergence of System of Systems correlated M&S to microelectronics architectures to help compress the development and verification cycle of complex systems.

Name: Michael Smith, Ph.D.
Title: Research Engineer - Hardware Technologies
Organization: Apple
Bio: Michael is a technical lead with the Hardware Technologies team responsible for Apple's industry-leading silicon designs. He has over 20 years' experience in consumer imaging systems, data analytics, and emerging education programs. Prior to Apple, he held technical leadership roles with Intel and France Telecom R&D. During his breaks from industry, he has held leadership roles in engineering research at academic institutions worldwide... Michael received a B.S. degree in electrical engineering from Tuskegee and North Carolina A&T State University, a M.S. in electrical engineering from Stanford University, and a Ph.D. in computer engineering from Carnegie Mellon University.

Name: Sonya Smith, Ph.D.
Title: Professor and Executive Director of the RITA UARC
Organization: Howard University
Bio: Dr. Smith obtained her Ph.D. in Mechanical and Aerospace Engineering from The University of Virginia (UVA) and was the first African American woman to do so. She joined the Howard University faculty that same year and is the first female Professor in the Department of Mechanical Engineering. Dr. Smith has established an interdisciplinary theoretical and computational research laboratory entitled the Applied Fluids-Thermal Research Laboratory (@FTERLab). Her expertise is in developing customized simulations for a variety of engineering applications. Current projects include thermal management of electronic packaging in fixed-wing, UAV and space vehicles, as well as modeling and simulation of biomechanical systems. She has received support for her research from NSF, NIH, NASA, DOD, and industry. Dr. Smith is a Fellow of the American Academy of Arts and Sciences, a Fellow of the American Society of Mechanical Engineers (ASME), and an Associate Fellow of the American Institute of Aeronautics and Astronautics (AIAA). Her memberships in other professional societies include, the American Astronautical Society(AAS), Association for the Advancement of Artificial Intelligence (AAAI), and the American Geophysical Union (AGU). She also a Fellow and past President of Sigma Xi: The Scientific Research Honor Society. As an experienced scientist and engineer, Dr. Smith's personal goal is to be a mentor and resource for students and young faculty/professionals in STEM.

Name: Dinadayalane Tandabany
Title: Professor, Chemistry
Organization: Clark Atlanta University
Bio: Dr. Dinadayalane Tandabany is a full Professor in Department of Chemistry at Clark Atlanta University (CAU) and received multiple grants from NSF and Department of Energy (DOE). He mentored and advised several undergraduate and graduate students including Ph.Ds. His research contributions are in carbon-based nanomaterials and 2D materials including hybrid systems toward the applications in alternative energy, semiconductors, chemical and biosensors. He has co-authored more than sixty (60) peer-reviewed articles and several book chapters that received 2500+ citations with an

h-index of 28. He is the Series Editor of Theoretical and Computational Chemistry book series published by Elsevier. He was awarded the 2019 STEM Innovator Award by BEYA.

Name: Donnell Walton, Ph.D.
Title: Deputy Director, RITA UARC
Organization: Howard University
Bio: Donnell Walton, an industrial physicist with 25 years of experience, has transformed research concepts into market products. His expertise spans optical communications, biological sensors, high-power lasers, consumer electronics, and wireless technology for autonomous vehicles. Walton's contributions are documented in over 24 US patents and more than 100 articles and presentations. He is the deputy director of the RITA UARC at Howard University and an adjunct professor at Cornell University. Previously, he led the Corning West Technology Center, fostering partnerships and exploring tech markets. Walton was a physics professor at Howard University, earning an NSF CAREER grant. He is active in various professional societies and is a Fellow of the American Physical Society and the National Society of Black Physicists.

Name: Talitha Washington, Ph.D.
Title: Executive Director, Center for Applied Data Science and Analytics
Organization: Howard University
Bio: Dr. Talitha Washington serves as the Executive Director of the Center for Applied Data Science & Analytics, the Sean McCleese Endowed Chair in Computer Science, Race, and Social Justice, a Professor of Mathematics, and co-chair of the AI Advisory Council at Howard University. Dr. Washington serves as the Past-President of the Association for Women in Mathematics (AWM) and previously served as a Program Director at the U.S. National Science Foundation (NSF). She is a Fellow of the AWM, the American Mathematical Society (AMS), and the American Association for the Advancement of Science (AAAS).

Name: Aurelia T. Williams, Ph.D.
Title: Special Advisor to the President & Senior Vice Provost
Organization: Norfolk State University
Bio: Dr. Aurelia T. Williams is a transformational leader at Norfolk State University (NSU), serving as Special Advisor to the President, Senior Vice Provost for Academic and Faculty Affairs, Executive Director of the Cybersecurity Complex, and Professor of Computer Science. With over 20 years of experience, she has enhanced NSU's Cybersecurity initiatives, securing $42 million in funding. As a former Chair of the Computer Science Department, her leadership fostered collaboration and student success. A lifetime member of the Norfolk State University Alumni Association, she was named a Distinguished Alumni in 2024 and recognized as one of CoVABiz's 150 Most Influential People in Coastal Virginia.

Name: Michelle Williams
Title: Executive Director
Organization : Semi Foundation
Bio: "Michelle Williams is the Executive Director of the SEMI Foundation. Michelle oversees the organization's strategy, communications, growth, and partnerships with government workforce development investments in the microelectronics industry. Michelle has supported the launch and scaling of major initiatives and secured significant funding for programs that support industry awareness and welcome all people into industry careers. She is an accomplished strategist, writer, and speaker who has presented to national and global audiences on workforce development and organizational culture. Previous to SEMI, Michelle spent 15 years at the helm of nonprofit organizations dedicated to strengthening communities through creative problem-solving and cross-sector partnerships.

ABSTRACTS

APPLICTIONS AND SUSTAINABILITY

Advancing Semiconductor Education Through NSF-Funded Collaborative Research
Presenter's Name: Suxia Cui
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Institution: Prairie View A & M University

Coauthors: Mohammadreza Hadizadeh, Zhigang Xiao, Mubbashar Khan, Satilmis Budak, Xiang Zhao, Qunying Yuan, Shujun Yang, Lujun Zhai

The Chips & Science Act, primarily focused on enhancing semiconductor production, also presents significant opportunities for workforce development. Prairie View A&M University (PVAMU), Central State University (CSU), and Alabama A&M University (AAMU) have all received industry funding to strengthen their teaching and research capabilities in semiconductor design and manufacturing. However, minority-serving institutions face persistent challenges, including limited access to proper training, sustaining costly tapeout projects, and adequately assessing the impact on their communities. Without addressing these barriers, underrepresented communities will face the risk of being left behind in future opportunities stemming from the Chips & Science Act.Therefore, PVAMU, CSU, and AAMU are collaborating to seek solutions and raise nationwide awareness of the aforementioned problems. The team secured $1 million in NSF funding to tackle the semiconductor workforce shortage through comprehensive education initiatives. These initiatives cover the entire chip manufacturing process, including materials science, IC design, fabrication, and testing. The education and outreach activities include: (1) building collaboration partnerships among three institutions across three states; (2) enhancing semiconductor curricula with the focus on historically marginalized communities; (3) training future leaders through seminars and workshops; (4) developing and advocating certificate programs that equip the workforce with emerging semiconductor techniques; and (5) supporting students with scholarships and internships through industry connections. Through this project, our team aims to share experiences with peer researchers and educators, fostering discussions on best practices and pathways for semiconductor workforce development at minority-serving institutions.

VLSI CHIP DESIGN AND FABRICATION FOR SOLAR PANEL DIAGNOSIS SYSTEM
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Solar power is widely utilized as a renewable energy source, capturing sunlight to generate electricity. As global fuel reserves are anticipated to deplete within the next 50 years, the demand for renewable alternatives like solar energy is escalating. It is currently among the most favored choices, employed on rooftops and expansive solar fields where clusters of panels are installed. However, when a few panels within these clusters malfunction, it becomes challenging for most individuals to pinpoint the issue. This highlights the necessity of a specialized chip capable of identifying problems within groups of solar panels, ensuring the uninterrupted operation of our renewable energy systems. To detect malfunctioning panels in a cluster, a tiny chip is designed and attached to a solar panel. A 32-pin chip is developed, incorporating voltage-sensing and current-sensing circuits, along with logical blocks that generate an alert when an open or short circuit occurs in the solar panel. A memory unit with a reset button is also included in the circuit. So, until the problem is resolved, the alarm indicator remains on. The designs were implemented in Cadence Virtuoso IC 6.18 and the Layout Suite using TSMC 180 nm technology for tapeout. The schematic design, layout design, error testing were successfully completed. Functional components were tested and verified through the ADE L environment. LVS and DRC error tests were successfully completed using Assura. A 32-pin pad frame was designed and connected to the corresponding pins.

Immersive Virtual Reality-based training to perform the photolithography process
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Coauthors: Dickson Afful, Michael Kozhevnikov

This research focuses on developing an immersive Virtual Reality-based Training Environment (VRTE) for photolithography, addressing the challenges of traditional practical training, such as high costs and injury risks. The research contributes to professional training and workforce development in the semiconductor industry. As the industry increasingly relies on advanced technologies, integrating VR into training programs

provides early exposure and hands-on experience with these platforms, enhancing the workforce's skills and readiness. Immersive VR technology offers a more engaging and active learning experience, ensuring greater motivation and understanding among trainees. VR training is inexpensive, injury-free, easily adjustable, scalable, and can be conducted remotely. VR environments are easy to supplement, strip, or change, allowing one system to train for several processes, thus saving costs. The immersive VRTE prototype for photolithography is designed and prototyped using the Unity development platform. The developed version is a high-fidelity VRTE and already features full-scale navigation within the 3D space and controller integration for effective interactions. Currently, the following parameters of the prototype module are analyzed: (a) Realism and Authenticity: creating realistic and contextually accurate environments can enhance the learning experience and make it more relevant to real-world applications; (b) Presence and Immersion: techniques such as realistic avatars and environmental interactions can enhance this feeling; (c) User Interaction: evaluating the effectiveness of controllers in enhancing user engagement and interaction; (d) E-Learning: analyzing the quality and comprehensiveness of module activities and scaffolding features, including levels, quizzes, and animations; (e) Accessibility: ensuring the module is accessible across multiple platforms and devices.

Growing the Computer Engineering Workforce through the CStoCMPE Program

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Coauuthors: Laura Haynes

The CStoCMPE Program is a strategic academic partnership between Morehouse College and Georgia Tech, designed to provide Morehouse Computer Science majors with the opportunity to pursue dual degrees in Computer Science and Computer Engineering. Through cross-enrollment, students will take Computer Engineering courses at Georgia Tech while completing their Computer Science degree at Morehouse. Transportation to Georgia Tech for approved courses will be provided by Morehouse, ensuring seamless access to educational resources. The program's structure enables students to major in Computer Science at Morehouse and transition into Georgia Tech's Computer Engineering program, which is ranked #5 overall and #2 among public institutions according to U.S. News & World Report. Georgia Tech will offer academic and professional development opportunities, while both institutions will collaborate on pre-college outreach and academic support to ensure student success. The curriculum covers key areas in Computer Engineering, including distributed systems, cybersecurity, hardware architectures, and robotics.The program aligns with national efforts to address the growing demand for skilled engineers, as highlighted by the CHIPS and Science Act, which allocates $52.7 billion to strengthen U.S. semiconductor manufacturing and research. Industry estimates predict a shortage of 300,000 engineers by 2030, emphasizing the critical need for programs like CStoCMPE.Supported by NSF grants (NSF #2332411, NSF #2318703), this initiative aims to build a sustainable pipeline for underrepresented students into computing and engineering fields. For more information, students can access interest forms and meeting slides through the provided resources.

Providing Leading Edge Process Technology and Test Chip Opportunities to Universities

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Organization: Intel

As chip manufacturing has become more and more advanced, universities have needed to rely on external manufacturing to manufacture their test chips. Intel's University Shuttle Program has been a key partner in facilitating the fabrication of university designed test chips and helping educate students on taping out a chips on leading edge process nodes. In this talk we will go over the USP's work supporting test chip and class tapeouts on Intel 16 and future plans for the program's transition to Intel 18A.

Building the Semiconductor Workforce: Nanomanufacturing Training for Veterans at HBCUs

Presenter's Name: Thong Le
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Coauthors: Hargsoon Yoon, Patricia Mead

Norfolk State University (NSU), in collaboration with Penn State University (PSU) and Tidewater Community College (TCC), has been at the forefront of expanding workforce education in semiconductor manufacturing through the Nanomanufacturing Certificate Program (NCP) for Veterans. Launched in 2021, this 12-week intensive training program equips military veterans and transitioning personnel with nanotechnology-based manufacturing skills critical to the semiconductor industry. The program integrates lectures webcast by Penn State University, hands-on cleanroom training at the Micron-NSU Nanofabrication Cleanroom, and recruitment support from TCC, ensuring a robust learning experience. To further advance semiconductor workforce readiness, NSU has extended its efforts with the Microelectronics and Nanomanufacturing for Veterans (2022–2026), a structured sequence of six courses (each equivalent to 3 credits) that provide a comprehensive blend of theoretical knowledge and practical laboratory experience. This program not only enhances participants' expertise in nanofabrication and characterization techniques but also prepares them to obtain American Society for Testing and Materials (ASTM) International certifications in nanotechnology. As a Historically Black College and University (HBCU), NSU's leadership in semiconductor workforce development underscores the vital role of HBCUs in shaping the future of the U.S.

semiconductor industry. By leveraging partnerships and state-of-the-art facilities, the program creates pathways for military veterans to enter and excel in semiconductor manufacturing careers. This initiative aligns with national efforts to strengthen the domestic semiconductor workforce, addressing the industry's pressing talent shortages while fostering diversity and innovation.

Collaborative Interactive Data Science Academy
Presenter's Name: David Lockett
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This innovative summer program for high school students that combines data science, robotics, and NASA's geospatial and extraterrestrial data using Virtual/Augmented/Mixed Reality (VR/AR/MR) technologies. Developed by Meharry Medical College's School of Applied Computational Sciences and Fisk University, this 2-week residential experience aims to stimulate curiosity in data science and emerging technologies while building critical thinking skills and diversifying the next generation of STEM professionals. Students will engage in hands-on activities using state-of-the-art VR/AR/MR systems to interact with NASA data and virtual objects in a collaborative, game-like environment. They will work on real-world challenges, such as designing a path for a Mars robot to assist NASA Ingenuity. The program incorporates various STEM disciplines, including computer vision, robotics, remote sensing, cybersecurity, and machine learning. Activities include 3D modeling from smartphone and quadcopter imagery, astronomical observations, and field trips to STEM career organizations. NASA and industry experts will provide presentations, offering insights into potential career paths. The program, running from 2023-2027, aims to increase STEM awareness, prepare students for undergraduate STEM degrees, and create pathways to graduate studies in data science. By providing unique on-campus research experiences and promoting individual and team learning, this summer academy seeks to inspire and equip the next generation of data scientists, researchers, and explorers with the skills needed to address future challenges in terrestrial and extraterrestrial environments.

SEMI Foundation's National Network for Microelectronics Education (NNME): Program Details and A Call for Participation
Presenter's Name: Michelle Williams
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Organization: The SEMI Foundation

The SEMI Foundation has been selected to be the operating Hub for the new National Network for Microelectronics Education (NNME), which will will open the door for more opportunities, more training, and more connection with industry to ensure that Americans have the training for the skilled jobs of today and tomorrow. The Hub will establish Regional Nodes across the country, each with its own programs and centers, to offer consistent, rigorous, engaging curricula, instructional materials, experiential opportunities, teacher professional development and more. The Hub will also aggregate updated and modernized curricula for dissemination nation-wide, and conduct an extensive microelectronics industry awareness campaing. Join this session to learn about the NNME, the involvement of the HBCU CHIPS Network, and how your institution can engage with and participate in this important opportunity.

MATERIALS & FABRICATION

Synthesis andCharacterization of Platinum (II) Ethylenediamine complexes with Thioures-like Ligands
Presenter's Name: Ashwaq Bahkali
Classification: Graduate Student
Research Category: Materials & Fabrication
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Institution: Texas Southern University

This study focuses on the synthesis and characterization of platinum(II) ethylenediamine complexes with thiourea-like ligands, targeting the development of improved anticancer drugs. Cancer remains a global health concern, and platinum-based drugs, particularly cisplatin, have played a key role in cancer treatment for decades. However, the limitations of cisplatin, such as severe side effects and low water solubility, have led researchers to explore new platinum-based compounds with better efficacy and reduced toxicity. In this work, 15 novel platinum(II) complexes were synthesized and characterized. These complexes follow the general formula [Pt(en)L2](NO3)2, where "en" represents ethylenediamine and "L" is thiourea or one of its derivatives, such as 1-benzyl-2-thiourea, 1-cyclohexyl-2-thiourea, and others. The complexes were synthesized via a reaction involving [Pt(en)(H2O)2](NO3)2, produced in situ by treating Pt(en)I2 with silver nitrate and adding two equivalents of the desired thiourea derivative. Characterization was performed using elemental analysis, IR spectrometry, and NMR spectroscopy. Additionally, the crystal structures of five of these complexes were determined using single-crystal X-ray diffraction, revealing the monoclinic and orthorhombic space groups of the compounds. These new platinum(II) complexes are water-soluble, a crucial feature for potential therapeutic applications, making them promising candidates for further investigation in the development of more effective anticancer treatments.

Chalcogenide semiconductor nanomateroals for reconfigurable photonics: from materials, mechanisms to applications
Presenter's Name: Joshua Burrow
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Institution: Morgan State University

Coauuthors: Thomas Searles, Imad Agha, Andrew Sarangan

We present a bottom-up growth approach to realizing intrinsically chiral chalcogenide nano-helices, achieving high-speed control of optochirality. Utilizing the non-volatile transition of $Ge_2Sb_2Te_5$ (GST) nanopatterned medium, we demonstrate polarization modulation exceeding 50,000 cycles. This advancement represents a significant step toward dynamic photonic devices with rapid and reversible control, offering potential applications in optical communication, sensing, and chiral light-matter interactions.

Ge-Si Alloy Microbolometer Fabrication Process
Presenter's Name: Daemar Casey
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Coauthors: Mukti Rana

Bolometers are devices used to measure the power of incident electromagnetic radiation by heating a material where electrical resistance changes depending on temperature. A microbolometer is used as a thermal camera detector, where infrared radiation between 7.5um-14um targets the detector's material, heating it to change its electrical resistance. The change in resistance is processed into temperatures and used to create an image. The microbolometer fabrication process follows the depositing of multiple layers of elements from Aluminum, Ge-Si Alloys, and Ni-Cr through PVD deposition, Photolithography, and Plasma ashing. Fabricating the Ge-Si alloy microbolometer creates six layers. The mirror layer, sacrificial layer, pads and contacts layer, arms layer, sensing layer, and absorbing layer. Results presented 187 nm, 400nm, and 210nm thicknesses for the mirror, pads & contacts, and arms layers. Sputter deposition operations ran parameters at a deposition pressure of 5.04E-03 and 25C for the temperature. Photolithography operations ran with parameters at average dosages of 66.78 (J/cm^2). Plasma ashing operations ran with parameters at 200W with pressure at 1mTorr. Future studies will focus more on streamlining the fabricating of Ge-Si alloy microbolometers.

Growth of Nanostructure gallium nitride (GaN) thin films for the Application of Electronic Materials
Presenter's Name: Baraka Chimba
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Institution: Alabama A &M University

Coauthors: Sydney Fleming, Satilmis Budak, Shujun Yang, Xiang Zhao, Qunying Yuan

We report the growth of nanostructured gallium nitride (GaN) thin films and fabrication of GaN–based electronic devices. Nanostructured GaN thin films will be grown as the active semiconducting channel material for the fabrication of GaN-based field-effect transistors using plasma-enhanced atomic layer deposition (ALD). GaN–based electronic devices such as GaN field-effect transistors and inverters will be fabricated with the ALD-grown GaN film using the clean room-based micro- and nano-fabrication techniques. Trimethyl gallium (TMGa, Ga(CH3)3) precursor will be used as the Ga source and ammonium (NH3) gas will be used for the growth of semiconducting GaN thin films. The GaN thin films will be analyzed by scanning electron micrograph (SEM) and energy-dispersive X-ray spectroscopy (EDS). The electrical property of the fabricated GaN devices will be measured. The characterization results of the nanostructured Gan thin films and the measurement results on the fabricated GaN–based electronic devices will be reported in the HBCU CHIPS Network Conference.

Intrinsic Antiferromagnetic topological insulators
Presenter's Name: Sugata Chowdhury
Classification: Junior Faculty/ Lecturer/ Instructor
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Institution: Howard University

The concept of electronic topology and the associated topological protection brings great opportunity for developing next-generation spintronics devices, especially those requiring minimal scattering or high quantum mechanical coherence properties. Among the different classes of topological materials, the 2D-antiferromagnetic topological (2D-AFMTIs) materials have attracted enormous attention. Magnetism in 2D-AFMTIs affords many opportunities to interplay with and tune the topology and, thus, the functionality of these materials - bringing dissipationless Quantum Anomalous Hall Effect (QAHE) physics, quantum spin liquid states, etc. This great promise has not, however, been properly realized so far at elevated temperatures because of the lack of ideal 2D-AFMTIs. Here, we will focus on newly synthesized MnBi2Se4 family and UOTe. The exotic quantum states of bulk and layered UOTe and MnBi2Se4 family will unlock the complex dependence of topological phases on fundamental electronic and structural parameters and explain how to modify these parameters through strain, doping, or change in geometry to maximize material performance.

Anisotropic Magnetic Entropy Changes in Single Crystal CrSBr
Presenter's Name: Anirban Goswami
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Coauthor: Zdenek Sofer

CrSBr is a layered van der Waals material with unique magnetic properties, attracting significant research interest. In this study, we examined the magnetic behavior of a single-crystal CrSBr sample, synthesized using the two-zone chemical vapor transport (CVT) method. Testing revealed a rapid shift in the peak temperature of the magnetic entropy change as the magnetic field increased: from 132 K at 0.1 T to 170 K at 9 T for the in-plane direction, and from 132 K at 0.1 T to 159 K at 9 T for the out-of-plane direction. This indicates strong magnetic interactions within the layers above the Néel temperature (TN = 132 K). Analysis of relative cooling power (RCP), the full width at half maxima of the magnetic entropy peak (δTFWHM), and the critical exponents showed that CrSBr transitions between magnetic states in a way consistent with three-dimensional behavior. These findings highlight the potential of CrSBr for intriguing magnetic properties and its importance in studying layered magnetic systems.

Design, Fabrication, and Characterization of Thermoelectric Devices
Presenter's Name: Kristen Harris
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Institution: Alabama A & M University

Coauthors: Essence Carter, Cole Cooper, Zaria Weeks, Satilmis Budak, Zhigang Xiao

Dr. Zhigang Xiao and Dr. Satilmis Budak are working on this project to fabricate high-efficiency thermoelectric materials and integrated devices for the application of power generation and solid-state cooling using the clean room-based standard semiconductor fabrication processes and train students to perform the fabrication processes and experiments. To fabricate integrated thermoelectric (TE) devices with the nano-layered super-lattice thin films using the standard semiconductor microfabrication, the following steps were performed: 1) To support the workforce development, four students were trained on clean room fabrication process and safety trainings. 2) Students were trained to operate e-beam deposition system to grow thin films using the crucibles. 3) Initial growths were performed on Bi2Te3 and Sb2Te3, and Bi2Te3/Sb2Te3 thin films for characterizations. 4) Students were trained on the characterization instruments including thin film thickness measurement, thermal treatment furnace, four probe van der Pauw measurement system for resistivity, mobility, density, sheet resistance, Hall effects and type of carrier measurements. 5) Students have been trained on the other techniques related to the fabrication and characterization procedures. 6) After students reach the efficient data for the thin films, they will be trained on fabrication of the thermoelectric devices using the microfabrication and characterization techniques. The results will be shared during the HBCU Chips Annual meeting.

Scandium Diboride Semimetallic Single Crystals by Laser Floating Zone Method
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Institution: Morgan State University

Coauthors: Ahamed Raihan, Astrid Kengne, Satya Khushwaha, TYrel McQueen, Michael Spencer, MVS Chandrashekhar

Scandium diboride (ScB2) is a semi-metallic ultrahard ceramic that is lattice matched to ultra-wide bandgap (UWBG) AlGaN. Given the very high melting point of these ultrahard transition metal diborides, synthesis is challenging, leading to few reports of synthesis of single crystals despite the large body of work on their application in ceramic composites. This lattice match of ScB2/Al0.55Ga0.45N would reduce the strain and crystal defects of epitaxial layers for high voltage vertical power devices >5kV. Here, we demonstrate the growth of ScB2 crystals using a floating zone melting growth technique known as the laser-diode floating zone (LDFZ) method. Polycrystalline ScB2 rods were used as our feed and seed rods. Metallic Scandium was used as a flux to lower the melting point at an argon pressure of 5atm. Our growth rate is ~2mm/hr or ~10x faster than the only other report of ScB2 single crystals. The crystal grew until all the Sc flux was absorbed by the feed rod and the molten zone eventually separated, giving a typical total growth of >20mm,. After cutting into slices using a diamond wire saw, X-Ray Diffraction (XRD) data shows clear signatures of (001) ScB2 while Laue patterns show six-fold symmetry over mm length scales. A four-point probe measurement showed a bulk resistivity ~10μΩ-cm, or ~5x lower than metallic scandium, and over 100x lower than conducting SiC/GaN, showing the promise of this lattice matched substrate for vertical AlGaN power devices, effectively eliminating the substrate series resistance component of the on-resistance in UWBG devices.

Simulation of Surface Barrier and its Effect on Betavoltaic Battery
Presenter's Name: Monté Hendrix
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Coauthors: Kishak Cinfwat

Betavoltaic power sources are semiconductor-based devices that convert beta radiation into electricity. These devices, which utilize radioactive isotopes to emit beta particles, are influenced by several factors such as the energy of the emitted particles, the absorption properties of the semiconductor material, and the efficiency of charge collection. A key issue in improving the performance of betavoltaic devices is the impact of surface defects and dangling bonds, which can trap charge carriers and act as recombination centers, leading to non-radiative recombination. This decreases the efficiency by increasing scattering and reducing charge carrier mobility. In this study, we investigate the effect of surface depletion on the efficiency of a PN Gallium Nitride (GaN) betavoltaic device, specifically focusing on the P+ layer. We performed a sweep of layer thicknesses ranging from 3 to 300 nm at doping concentrations of 1E18, 1E19, and 1E20 cm^-3. The results reveal an inverse relationship between the short-circuit current and both the thickness and doping concentration of the P+ layer. Thinner layers and higher doping concentrations reduce the ability of the device to efficiently collect charge carriers, likely due to increased surface recombination and reduced electric field strength. Our findings highlight the critical role of surface defects and depletion region characteristics in optimizing betavoltaic device performance, providing insights for future improvements in design and material selection for enhanced efficiency.

Recent Advances in Development of 4H-SiC for Microelectronics
Presenter's Name: Ningxin Li
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4H-Silicon Carbide(4H-SiC) is the representative of the third-generation semiconductors and a monocrystalline material that exhibits exceptional properties, including a wide bandgap, high thermal conductivity, and low intrinsic phononic dissipation. These characteristics make 4H-SiC highly suitable for harsh environment microsystems, enabling reliable operation under extreme conditions such as high temperatures, voltages, intense radiation, and strong vibrations. Despite these advantages, the immaturity of its device nanofabrication—particularly the precision etching process—remains a significant challenge for 4H-SiC's widespread adoption and potential replacement of traditional silicon wafers. The strong chemical inertness of SiC makes it difficult to etch, and achieving high-precision etching remains a formidable obstacle in the fabrication of SiC-based Micro-Electro-Mechanical Systems (MEMS) devices, such as resonators and gyroscopes. This study presents significant advancements in high-aspect-ratio deep reactive ion etching of 4H-SiC. Utilizing an electroplated nickel mask, we successfully achieved aspect ratios ranging from 10:1 to 21:1 in deep trenches with critical dimensions between 1–10 μm, with an 88.5° tapering angle, and sidewall roughness below 200 nm. Depth uniformity across the wafer remained within ±0.85 μm (~2%), enabling batch fabrication of 4H-SiC MEMS devices with exceptional performance potential. Moreover, the fabricated 4H-SiC disk resonators were characterized to show a small 5Hz frequency split and a high-quality (Q) factor approaching 5 million at room temperature. These advances etching results in wafer-level mark a pivotal step toward scalable manufacturing of ultra-high-quality SiC micro-resonators used for demanding working environments, further unlocking the potential of 4H-SiC for next-generation MEMS applications.

Photoluminescence of Nanoscale Semiconductor Materials
Presenter's Name: Zhiping Luo
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Semiconductors possess unique electronic properties characterized by transitions within narrowed bandgaps, typically ranging from 0 to a few electron volts (eV), making them highly suitable for lighting applications. As global energy consumption continues to rise at an unprecedented rate, energy-saving strategies have become increasingly crucial to mitigating environmental impact and reducing economic costs. Lighting alone accounts for over 15% of the world's total electricity consumption, yet conventional lighting technologies remain inefficient, leading to significant energy waste. To address these challenges, extensive research has been directed toward developing light-emitting diodes (LEDs), which offer superior energy efficiency, longer operational lifespans, and enhanced brightness compared to traditional lighting sources. Our study investigated the luminescence properties of vacancy-ordered hexagonal perovskite Cs_2MF_6 (M = Ti, Zr, Hf, and Sn) doped with Mn, a promising class of materials for phosphor applications. The materials were synthesized through controlled chemical reactions, ensuring high purity and reproducibility, and were subsequently characterized using X-ray diffraction and electron microscopy to analyze their structure and morphology. Mn doping was optimized based on photoluminescence characteristics, allowing for the tuning of emission properties and enhancing quantum efficiency. Further spectroscopic studies were conducted to evaluate energy transfer mechanisms and thermal stability, which are critical factors for real-world LED applications. Finally, the synthesized phosphors were integrated into phosphor-converted LEDs, demonstrating their potential as efficient and stable luminescent materials for next-generation lighting technologies.

Material Characterization and Fabrication of microbolometer with GeSiSnO sensor using surface micromachining.
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Our research of Ge-Si-Sn-O thin films as a bolometric material will contribute to the development of more sensitive imaging systems. High TCR, low thermal conductance and higher absorption in the wavelength of interest are crucial in determining the responsivity of the sensing material. The work presented investigates the Sn doped GexSi1-xOy film for desired electrical thermal and optical properties for using it as NIR (SWIR) and mid IR sensor in microbolometer. Characteristic properties presented include TCR (0.0326/K),Optical Band Gap (1.06eV) ,Activation energy and 1/f Noise of $2.28 \times 10{-}12$ V2/Hz at 10 Hz frequency for a bias current of 1 μA, for Ge0.45 Si0.05 Sn0.15 O0.35 film as thermal sensor in uncooled microbolometer. In our sensor, we minimize heat loss by suspending the sensing layer from the substrate by using a polyamide sacrificial layer. The fabrication is done on a Si/Si3N2 substrate. We used lift-off to pattern the layers of the bolometer. For the infrared mirror, we patterned it by first spin coating Futurrex NR9-1500PY negative photoresist, baking, exposing with UV light, developing in Futurrex RD6, and lastly aluminum deposition via sputtering. The photoresist is then removed using Futrrex RR5. HD Microsystems PI-2610 polyamide was used for the sacrificial layer. It was spin coated, cured, and patterned using oxygen plasma ashing. The electrode, sensing, and absorber layers were deposited and patterned using the lift-off process. Plasma ashing is used to remove the remaining polyamide to suspend the sensing layer.

Demonstration of TCAD Modeling for GaN Devices
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Gallium Nitride (GaN) is a semiconductor material of which current knowledge is limited compared to more abundant, Silicon-based semiconductors. In order to add to our understanding of GaN, we aim to create a predictive room temperature GaN Schottky diode simulation model utilizing Silvaco Technology Computer-Aided Design's (TCAD) physical simulator. I-V data taken from fabricated GaN Schottky diodes serve as the basis for our preliminary simulation comparison based upon GaN based physical models. From there I-V data from Circular TLM (CTLM) structures and C-V data allowed for the extrapolation of a Schottky barrier height and specific contact resistivity and these parameters were implemented into our final simulation. Through this investigation, it was discovered that a 2-D simulation structure, with equivalent area to a physical structure, can generate an I-V characteristic with an agreeable threshold voltage to the measured I-V characteristic. Further analysis is needed to resolve the discrepancies between specific onresistance of the simulated and measured devices. Our research serves as a starting point in creating predictive simulation models in Silvaco TCAD which can be used to understand the physical phenomena which occur in GaN Schottky diodes.

Growth of TMDs and their heterostructures for next generation device applications
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Silicon has long been a foundational material in the semiconductor industry, primarily because of its excellent electronic properties and abundant availability. However, as electronic devices become more compact and the demand for higher performance increases, exploring alternatives to silicon-based semiconductors is essential, as silicon is reaching its limits. The challenges encountered at the nanometer scale, such as increased leakage currents, reduced gate control, and heat dissipation issues, present exciting opportunities for innovation. By proactively addressing these challenges, we can drive the development of advanced materials and technologies that will empower the next generation of semiconductors. Layered transition metal dichalcogenide (TMD) semiconductors, including molybdenum disulfide (MoS2) and tungsten disulfide (WS2), possess high electron mobility and can be formed into atomically thin layers. These characteristics make them suitable for flexible and nanoscale electronics, potentially replacing current silicon-based devices. However, a significant challenge lies in the large-scale production of high-quality two-dimensional (2D) TMD layers. Advancements in growth techniques, including metal-organic chemical vapor deposition (MOCVD) and chemical vapor deposition (CVD), hold great potential for overcoming this challenge. This research aims to discuss the growth of TMDs and their heterostructures, their electronic and optoelectronic properties, and their roles in developing advanced semiconductor devices.

Growth of Cubic Boron Nitride by Plasma Assisted Chemical Vapor Deposition on Silicon, Silicon Carbide and Diamond Substates

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Cubic Boron Nitride (cBN) is an ultra-wide bandgap semiconductor that has many excellent material properties, including an indirect bandgap that allows N and P type doping, high-predicted breakdown field high predicted electron saturated high thermal conductivity and material hardness second only to diamond. In this work we report on the growth of cubic boron nitride using a custom designed Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor. The growth chemistry consisted of Boron Trifluoride (BF3), Nitrogen (N2), Hydrogen (H2) together with inert gases of Helium (He) and Argon (Ar) (to sustain the plasma). The growth was performed at growth pressures of 1-10mTorr and growth temperatures of 700-9000C. During the growth a bias voltage of -50V was applied to the substrate holder. The thickness of the BN films was measured as .1-.3um indicating a growth rate of 50nm to 100nm/hr. depending on the amount of BF3 flow. Energy Dispersive X-Ray analysis (EDX) was performed in an electron microscope on the grown substrates and on small commercial platelets used in cutting applications. The results from EDX study showed that B/N ratio of ~2:1 was present on all substrates on which growth was attempted. The surface morphology was studied using optical and scanning electron microscopes (SEM) as well as atomic force microscopy (AFM). Fourier Transform Infrared Reflectance (FTIR) measurements were made on all the samples. FTIR measurements on polycrystalline diamond substrates in the best cases showed a 100% cBN signature.

QUANTUM & PHOTONICS TECHNOLOGIES

Exploring the Nonlinear Hall Effect in Chiral Non-Centrosymmetric RuGaSi Systems

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Quantum materials (QMs) with chiral symmetry exhibit intriguing quantum phenomena, such as the topological Hall effect, planar Hall effect, and nonlinear Hall effect (NLHE). But the connection between chiral symmetry and different properties of QMs remains poorly understood. To address this, we carried out a systematic theoretical study to understand how chirality influences the NLHE in newly synthesized ordered Ru7Ga6Si6 and disordered Ru7Ga5.8Si6.2 structures. To overcome the computational challenges associated with disordered systems, we considered three ordered chiral structures: Ru7Ga6Si6, Ru7Ga10Si2 and Ru7Ga2Si10. Dynamical stability calculations reveal that Ru7Ga6Si6 and Ru7Ga10Si2 are stable and allow us to explore their electronic properties. Our finding indicates that Ru7Ga6Si6 is direct band gap semiconductor whereas Ru7Ga10Si2 exhibits metallic behavior. Furthermore, chiral space group analysis demonstrates that non-vanishing Berry curvature leads to a finite Berry curvature dipole moment (BCDM), ultimately inducing NLHE under a harmonically oscillating electric field. These results provide fundamental insights into the role of chirality in QMs, highlighting its impact on transport properties.

Disassembly Sequence Optimization using Quantum Random-Access Encoding

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Automated disassembly processes have the potential to enhance the recycling of end-of-life products radically, and thus, achieving efficient disassembly planning becomes critical for remanufacturing, enabling reuse, and improving the sustainability of recovery processes. Therefore, the problem of Disassembly Sequence Optimization (DSO), with a potentially vast combinatorial search space, is critical to advance the future of remanufacturing.

The present work explores formulating the problem of interest as a Quadratic Unconstrained Binary Optimization (QUBO), with appropriate penalties for incorporating feasibility constraints, to be solved using Quantum Approximate Optimization Algorithms (QAOA). Crucially, we leverage a Quantum Random-Access Encoding protocol to enhance the scalability of the solution algorithms and enable high-quality solutions through actual Near-term Quantum Processing Units (QPUs), successfully exploiting current hardware capabilities at enhanced capacity.

Optothermal Metrology of Phase Change Chalcogenide Thin Films
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Photonic Integrated Circuits (PICs) play a critical role in quantum photonics by enabling the miniaturization, integration, and scalability of quantum devices. They allow for the integration of multiple photonic circuit elements on a single chip and facilitate the creation and manipulation of quantum states. Nonlinear optical processes, such as spontaneous parametric down-conversion, can be implemented on a PIC to generate entangled photon pairs for quantum cryptography or quantum computing operations. The ability to create interference patterns and control photon polarization, phase, and temporality on a chip is crucial for quantum algorithms and quantum communication protocols. However, their widespread adoption faces a significant challenge: variability. Fabrication imperfections in circuit elements can lead to inconsistent optical properties and unexpected device behavior, such as phase mismatches and insertion losses. This variability undermines performance, reducing efficiency and reliability. Typically, active tuning mechanisms, such as electrical heaters and PN junctions, are incorporated to compensate for these errors. The addition of these components results in a larger device footprint and higher power consumption. Alternatively, heterogeneous integration of materials, such as Lithium Niobate and various Phase Change Materials (PCMs), has been introduced as a path towards non-volatile functionality in PICs, allowing for defect compensation without active tuning, large power requirements, or electrical component integration. We propose a co-design model for the heterogeneous integration of PCMs on SOI waveguides for tunable phase shifting in linear PIC components, allowing for post fabrication tunability in PICs.

Ultraviolet spectrum downshifting in polymer nanocomposite photonics thin films for the enhancement of optoelectronic devices
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We report on Photonic polymer nanocomposite thin films with ultraviolet (UV) spectrum down-shifting that can be transferred using the open-air multi-beam multi-target pulsed laser deposition (MBMT-PLD) on opto-electronic devices, such as photo-voltaic (PV) cells, for the enhancement of their performance. The nanocomposites were made of the space-grade polymer CORIN impregnated with nanoparticles (NPs) of rare-earth (RE) doped compound NaYF4: Eu3+. NPs had a peak of down-shifted photoluminescence (PL) at 623 nm and a PL quantum yield (PLQE) of ~ 50%. The enhancement of the coated PV cells was two-fold: (a) protection from harmful solar UV radiation and (b) the increase of the PV conversion efficiency. We describe the results of characterization of the NPs using dynamic light scattering, X-ray diffraction, and optical spectroscopy. The nanocomposite films were deposited on Silicon heterojunction (SHJ), Copper-Indium-Gallium-Selenide (CIGS) and inverted metamorphic multijunction (IMM) solar cells. The cells were exposed to 365-nm UV radiation from a light emitting diode (LED). The I-V characteristics of the cells were measured with a solar simulator using AM0 filter. The proposed films improved UV stability of all three cell types: the power degradation significantly slowed down, CIGSs (by half). The proposed films have great commercial potential, especially for the applications to space power.

High-Performance Computational Modeling of Excitons and Trions in 2D Semiconductors
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We present a computational study of excitons and trions in two-dimensional (2D) semiconductors (MoS_2, $MoSe_2$, WS_2, and WSe_2) using high-performance computing. By solving the Schrödinger equation in momentum space, we determine ground and excited-state energies and wavefunctions for two-body electron–hole (exciton) and three-body (trion) bound states. The two-body exciton problem is solved with the Lippmann–Schwinger method, while the three-body trion system is addressed using the Faddeev method. We developed a parallel Fortran toolkit to model three interacting particles with distinct attractive and repulsive interactions, enabling the calculation of exciton and trion binding energies and wavefunctions in both momentum and configuration spaces and revealing their geometric structures. Large-scale computations on Ohio supercomputer clusters ensure efficient and accurate numerical solutions for these quantum systems.

Machine Learning-Driven Solutions for 1D Quantum Systems
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This project presents a machine learning (ML) approach for solving the one-dimensional (1D) time-independent Schrödinger equation to determine ground and excited energy levels and wavefunctions for three benchmark systems: a particle in an infinite square well, a particle in a harmonic oscillator, and the 1D hydrogen atom. A neural network approximates the wavefunction, while a variational method is used to minimize the loss function via gradient descent to obtain the energy eigenvalues. Numerical results show excellent agreement with exact analytical solutions for these 1D models. Ongoing work extends this

methodology to two-dimensional (2D) quantum systems, including excitons in 2D semiconductor materials.

Quantum Corners: Improving Emergency Response with Smart Traffic Management and Quantum Sensors

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Specially in the Washington, DC area, emergency vehicles are subject to traffic as it is very common to see emergency vehicles halted behind various cars on highways or even side streets due to congestion issues. Smart traffic management works well to solve this issue as it implements Internet of Things (IOT) sensors to provide information for traffic analysis. While IOT sensors provide a great foundation for smart traffic management, system designers can migrate to quantum sensing technology to enhance precision in data collection.To address the problem of delayed emergency response, the goal is to design a sensing system that sends information to a smart traffic management system. This information will be relayed to a smart traffic management system to plan the best route for an emergency vehicle to travel. Once the ideal path is planned for the emergency vehicle, the system will then send notifications to surrounding vehicles to update their current GPS routes to redirect them away from the emergency vehicles path.To accomplish the original goal, this work uses an autonomous car as a testbed using a mixture of cutting edge and state of the art technologies. In this testbed, the objective is to perform a hardware acceleration of ORB-SLAM2 with a Graph Neural Network designed in Vivado HLS and implemented on an Intel Cyclone 10 at the edge. After completion, the final goal is to report how the previous mentioned cutting edge technologies can be used to design the quantum sensing system for improved emergency response.

Microfabrication of RF Antennas for Quantum Sensing Applications

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Radio frequency (RF) signals are frequently used in emerging quantum applications due to their spin state manipulation capability. Efficient coupling of RF signals into a particular quantum system requires the utilization of carefully designed and fabricated antennas. Nitrogen vacancy (NV) defects in diamond are commonly utilized platforms in quantum sensing experiments with the optically detected magnetic resonance (ODMR) method, where an RF antenna is an essential element. We report on the design, microfabrication, and optimization principles of coplanar RF antennas for quantum sensing applications. Several novel coplanar waveguide (CPW) and microstrip RF antennas were designed and fabricated with over -30 dB experimental return loss at 2.87 GHz, the zero-field splitting (ZFS) frequency of the negatively charged NV defect in diamond. The efficiencies of the antenna were demonstrated in magnetic field quantum sensing experiments with NV color centers in diamond. An RF amplifier was not needed and the 0dB (1 milliwatt) output of a standard RF generator was adequate to run the ODMR experiments due to high efficiency of the novel RF antennas. This work constitutes a milestone towards miniaturization quantum sensing setups and realization of field portable quantum magnetometers.

Hybrid Quantum-Classical Approaches for Optimizing Disassembly Sequence Planning

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Disassembly is critical for sustainable recovery processes, enabling reuse, remanufacturing, and recycling of end-of-life products. This study explores a novel approach to Disassembly Sequence Optimization (DSO) by integrating Quantum Annealing with Quadratic Unconstrained Binary Optimization (QUBO) and Constrained Quadratic Model (CQM) formulations, leveraging CAD-based assembly designs to address computational challenges in industrial disassembly. Experimental results on two product designs demonstrated that the CQM formulation reduced disassembly costs while maintaining computational efficiency, whereas the QUBO formulation exhibited superior scalability for larger problem instances. These findings highlight the potential of quantum-assisted heuristics to enhance industrial disassembly planning. Future research should focus on refining hybrid quantum-classical methods to optimize resource allocation, improve efficiency, and adapt to diverse manufacturing scenarios. As quantum hardware advances, these approaches could revolutionize sustainable manufacturing by enabling more cost-effective and scalable disassembly strategies.

Photonic Integrated Circuits and Photonics Chips – Materials and Devices for Next Generation Silicon Platforms

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Abstract: Photonic Integrated Circuits (PICs) and Photonics chips are at the forefront of next-generation computing, quantum information, sensing, and communication technologies. However, key challenges

in achieving low-loss functionality, robust scalable generic component design, and compact device architecture are required to unlock their full potential. In this talk, we present our group's cutting-edge research in optical materials and photonic devices. simulation, Our work explores novel approaches for advancing Silicon-on-Insulator photonic platforms, including the development of on-chip nonlinear Mach-Zehnder Interferometers (MZIs), inline resonators, photonic metasurfaces. We also explore emerging optical materials the support strong light-matter interactions such as low-dimensional quantum materials, optothermal phase-change chalcogenides, and germanium-tin light light emitters. Through strategic collaborations with National Laboratories and research institutions, we have developed a diverse array of innovative projects addressing critical bottlenecks in silicon photonics. This talk will highlight these advancements and their implications for the future of photonic chip technology and workforce development.

Magnetic exchange interactions in kagome metal KMn3Sb5
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The concept of electronic topology and the associated topological protection brings great opportunity for developing next-generation spintronics devices, especially those requiring high quantum-mechanical coherence properties. Among these, different types of topological kagome materials have attracted attention because they exhibit a wide range of exotic quantum states, such as charge density wave (CDW), chiral non-collinear magnetic orderings, etc. KMn3Sb5, a new ferromagnetic (FM) kagome material, belongs to the same family as well-known CDW kagome materials like AV3Sb5 (A = K, Rb, and Cs). Although FM-KMn3Sb5 was predicted to be a non-trivial topological material with considerable anomalous Hall response, the presence of strongly correlated Mn:3d valence electrons necessitate further examinations. Our first-principles density-functional theory (DFT+U) calculations unveil an A-type antiferromagnetic (AFM) order in KMn3Sb5, which is sensitive to the strength of the onsite Coulomb interaction parameter U. A tight-binding Hamiltonian is constructed to evaluate Heisenberg exchange-interaction parameters and unveil the magnetic configuration of this complex system. We further discuss the role of electronic correlations on the electronic structure of AFM-KMn3Sb5.

Accurate Quantum States of Two-Dimensional Dipole Defects
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Edge dislocations are crucial in understanding both mechanical and electrical transport in solids, and are modeled as linear distributions of dipole moments. The calculation of the electronic spectrum for the two dimensional dipole, represented by the potential energy $V(r,\theta) = p\cos\theta/r$, has been the topic of several studies that show significant difficulties in obtaining accurate results. In this work we show that the source of these difficulties is a logarithmic contribution to the behavior of the wave function at the origin that was neglected by previous authors. By taking into account this non-analytic deviation of the solution of Schroedinger's equation superior results, with the expected rate of convergence, are obtained. This task is accomplished by "adapting" general algorithms for solving partial derivative differential equations to include the desired asymptotic behavior. We demonstrate this methodology for variational principle calculations as well as finite difference based numerical computation.

TECHNOLOGY & DESIGN

Designing a 2kV GaN p-i-n Diode Considering the Photon Recycling Phenomenon
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Wide bandgap semiconductors, such as Gallium Nitride (GaN), are transforming high-power device applications due to their superior critical electric field strength and exceptional thermal conductivity compared to silicon. In bipolar devices, conductivity modulation is essential for achieving enhanced performance; however, GaN's inherently short carrier lifetime, predominantly caused by radiative recombination, presents a significant challenge for bipolar devices. Photon recycling, a phenomenon where photons emitted through radiative recombination are reabsorbed, generating additional carriers, offers a promising approach to improve conductivity modulation in GaN-based devices. This study explores the feasibility of leveraging photon recycling to enhance conductivity modulation in vertical GaN p-i-n diodes, employing SILVACO TCAD simulations to assess its impact. Both intrinsic photon recycling (IPR) and extrinsic photon recycling (EPR) mechanisms are evaluated for their influence on the effective carrier lifetime and specific on-resistance (RON,SP). Two device architectures are investigated: a baseline structure designed for standard performance and an optimized design targeting a 2000V breakdown voltage. Simulation results reveal that photon recycling significantly bolsters conductivity modulation,

particularly through EPR, which demonstrates the most substantial reduction in (RON,SP) under low forward voltage conditions. A factor of 1.03 improvements in RON,SP is demonstrated for the 2 kV device whereas the improvement factor for the device with 9 μm drift layer is in the range of 1.4 - 2.2. These findings underscore the potential of photon recycling as a novel strategy to overcome GaN's intrinsic material limitations for the medium voltage power devices.

Atomic Layer Deposition: A enabling technology
Presenter's Name: Shyam Aravamudhan
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Atomic Layer Deposition (ALD) is an ultra thin-film (CVD-like) deposition technique that enables precise control over film thickness, composition, and conformality at the atomic scale and at (fairly) low temperatures. Utilizing sequential, self-limiting chemical reactions, ALD allows the deposition of ultra-thin, uniform coatings conformally on complex three-dimensional surfaces, particularly high-aspect ratio structures. In this talk, I will discuss ALD as the enabling technology for many advanced applications including for current and future transistor nodes, memory, energy storage, catalysis and biomedical coatings.

Instinctual Neural Networks for Time Limited Edge Environments
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Neural networks are a marvel of computing technology allowing for the most recent technological boom in industry and academia. However, too often these neural networks are very large and take a significant amount of time to train and utilize. In edge computing, resources are very limited by the principle of SWaP-C. This necessitates a new paradigm of neural networks which are fundamentally instinctual and are built to "react" in a very limited amount of time. We have created several demonstrations showing how an instinctual approach to neural networks can provide an advantage in edge environments where every millisecond of compute time matters.

Attacks and Countermeasures for Deep Learning Accelerators
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The quantized DNN (QNN) model parameters make it feasible to deploy Machine Learning (ML)/Deep Learning (DL) models on resource constrained IoT devices due to their significant storage reduction for large models. However, such reduced precision techniques introduce increased vulnerability to bit perturbations and radiation-induced Single Event Upsets (SEUs) which may cause significant accuracy degradations. QNN accelerators implemented in FPGA platforms have been widely adopted in the AI cloud facilities and IoT devices due to their superior power efficiency compared to CPU or GPU platforms. Our investigation aims to assess the vulnerability profile of the QNN accelerators to bit perturbation attacks/errors and Single Event Upsets (SEUs) errors at each layer, as well as potential vulnerable points in the FPGA design flows and tool suites for different DNN accelerator implementations such as BNN-PYNQ, CHaiDNN and ML Suite tools.

Integrate Digital Twin with Hidden Markov Model for Semiconductor Chip Performance Evaluation
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Evaluating chip performance is crucial for ensuring reliability and efficiency in modern electronics, but it poses significant challenges due to the complexity of semiconductor processes and the need for precise, real-time analysis. The integration of Hidden Markov Models (HMMs) with Digital Twins presents a novel approach to the semiconductor chip performance evaluation. This talk explores the creation of a digital twin for a semiconductor chip, which serves as a virtual replica that mirrors the physical chip's behavior in real-time. By incorporating real-time data from embedded sensors, the digital twin provides a comprehensive view of the chip's operational status.The application of HMMs within this framework allows for the representation of various operational states of the chip, such as normal operation, minor faults, and critical failures. Training the HMM with historical data enables accurate prediction of state transitions and emission probabilities. This integration facilitates real-time monitoring, anomaly detection, and predictive maintenance by continuously comparing the predicted state from the HMM with the expected state in the digital twin.The proposed methodology offers significant benefits, including enhanced reliability through early fault detection, cost savings by reducing unexpected failures, and improved

performance optimization. Additionally, the feedback loop created by the digital twin and HMM insights inform better design decisions for future chip iterations. This approach leverages the strengths of both HMMs and digital twins to create a robust, data-driven solution for the semiconductor industry.

Modelling and Simulation of Multi-junction P+IN+ Alphavoltaic Nuclear Batteries

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Monté Hendricks, Peker Milas, Marc Litz, Michael Spencer

Nuclear batteries find applications in medical implants, niche sensing application and suit all extreme environments. Nuclear batteries made from alpha sources offer the potential of higher energy density if the damage to the charge collection structures could be mitigated to prolong operational lifetimes of the battery. It is well knownthat a degradation of minority carrier mobility occurs due to alpha irradiation induced defects. Typical alpha damage is largely concentrated at the end of the stopping range. In GaN, this is about 7-10 μm. In this study, the performance of a P+IN+, GaN based alphavoltaic device was simulated using Silvaco Atlas, a TCAD software, for different lengths of the diode's I-region: 0.5μm, 1 μm, 1.5 μm, 2 μm and for lifetimes (τ) :1e-2 - 1e-15s, which is correlated to the anticipated defect density within the device due to irradiation. The simulation results show the behavior of the devices agreed with theoretical understanding of PIN devices. From the battery performance indices: Isc, Voc and Pmax, the half power point occurred at 5.011e-10 – 5.011e-11s indicating points of significant device degradation. The batteries with 0.5 -1 μm I-regions produced the highest power, and the Voc did not change significantly with I-region length which implies analphavoltaic battery design employing multijunction devices, say 0.5 - 1 μm connected in series or parallel could be deployed to circumvent the effects of the end of range damage while allowing for a sufficiently long diffusion length to facilitate collection from one alpha source density.

MATTER: MULTI-STAGE ADAPTIVE THERMAL TROJAN FOR EFFICIENCY & RESILIENCE DEGRADATION

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As mobile systems become more advanced, the security of System-on-Chips (SoCs) faces increasing threats from thermal attacks. This research introduces a novel attack vector called the Multi-stage Adaptive Thermal Trojan for Efficiency and Resilience Degradation (MATTER). MATTER exploits weaknesses in Dynamic Thermal Management (DTM) systems by manipulating temperature sensor interfaces, leading to incorrect thermal readings that, in turn, disrupt the SoC's ability to manage heat effectively. Our experiments show that this attack can degrade the performance of DTM by up to 73\%, highlighting serious vulnerabilities in modern mobile devices. By exploiting the trust placed in temperature sensors, MATTER causes DTM systems to make poor decisions, \ textit{i.e.}, failing to activate cooling mechanisms when needed. This degrades system performance and threatens hardware lifespan. This paper provides a detailed analysis of MATTER and underscores the need for improved thermal management systems in SoCs.

FlexGuard: Dynamic Scoring \& Stochastic Routing for Balanced Security-Performance in 3D NoCs

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Security vulnerabilities in microelectronic systems, particularly Multiprocessor System-on-Chip (MPSoC) architectures, are becoming increasingly critical as hardware Trojans, fault-injection attacks, and cryptanalysis techniques evolve. Among these, 3D Network-on-Chips (3D-NoCs), a key interconnect solution in modern MPSoCs, are especially susceptible to Through-Silicon Via (TSV) access threats, covert attacks, and malicious packet manipulation. These vulnerabilities compromise data integrity, performance, and reliability, necessitating secure and efficient countermeasures.This paper introduces FlexGuard, a dynamic security framework that enhances system resilience while maintaining performance and availability. By integrating Security-Performance-Availability (SPA) scoring and stochastic source routing, FlexGuard mitigates hardware-level threats by intelligently diversifying packet paths and dynamically adjusting routing policies. Unlike traditional security mechanisms that degrade performance, FlexGuard employs lightweight security measures to prevent timing attacks, fault injections, and traffic analysis with minimal overhead Experimental results demonstrate that FlexGuard reduces the success rate of TSV fault-injection attacks by over 60%, improves packet delivery reliability by up to 40% under adversarial conditions, and maintains an average latency increase of only 8% for secure packets compared to baseline routing. As microelectronic systems grow in complexity, security must be integrated at the architectural level without sacrificing efficiency. FlexGuard provides a scalable, adaptive, and high-performance security framework for next-generation MPSoCs and 3D-NoCs, reinforcing their resilience against emerging hardware-level threats while ensuring efficient operation.

Anatomy of an Undergraduate System-on-Chip Tape-Out Class
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We present a one-semester course that introduces computer engineering and computer science undergraduate students to System-on-Chip (SoC) design principles and methodologies, open-source and commercial electronic design automation tools, and how to use them to take a design from register transfer-level (RTL) to physical layout culminating in a chip tape out at 16nm FinFet technology and create a foundation for future exploration of SoC design. The prerequisites for the course include Digital Logic Design, Microelectronic Circuits, and Computer Architecture. By taking this course, students will do the following: 1) build combinational logic circuits using transistors optimizing for delay and power; 2) build sequential logic circuits using clock and storage elements while understanding the trade-offs of the different clocking methods; Pre-Silicon Design of an SoC from RTL (e.g., Verilog) to place and route (PnR), verification (LVS) and test; and 3) determine system power, performance, and area while developing an intuition for the trade-offs between these parameters, and how to iterate on the design to optimize them. The SoC tape-out course runs during the Spring semester. We anticipate no more than 20 students in the course. Students will 1) build RISC-V and AI/Cryptographic accelerator processors; 2) build interfaces such as the universal serial bus (USB), universal asynchronous receiver/transmitter (URAT), and Joint Test Action Group (JTAG); and 3) determine system power, performance, and area while developing an intuition for the trade-offs between these parameters for optimization. Lastly, our blended learning environment will present a plug-and-play post-silicon validation framework to bring up the SoC.

Detecting Hardware Trojans in Manufactured Chips without Reference
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Hardware Trojans (HTs) pose a significant threat to the security and reliability of integrated circuits (ICs). Due to their rare activation and stealthy nature, detecting HTs is exceptionally challenging. These Trojans can leak sensitive information or even cause permanent damage to circuits. A major challenge with many existing side-channel analysis techniques is their reliance on golden chips as references, which are often difficult to obtain. To address this issue, we introduce a novel reference-free method for detecting hardware Trojans in manufactured ICs, using Gaussian Mixture Models (GMMs) and power side-channel signals.In our study, we conducted experiments on the AES-128 cryptographic algorithm with five hardware Trojans selected from Trust Hub. The results from testing five different hardware Trojans (HTs) inserted into the AES-128 cryptography algorithm showed accuracies of 99.62%, 99.39%, 99.99%, and 78.66% respectively, and with an average accuracy of 95.52%. The tampered AES-128 designs were synthesized and loaded into an Artix-7 Field Programmable Gate Array (FPGA), where power measurements were captured. The proposed method provides a probabilistic framework that assigns probability values to side-channel measurements to detect hardware Trojan activation, enabling a reliable determination of whether an HT has tampered with a manufactured design.Additionally, our approach uses both past and current operational data of a design as a self-reference to detect HT activities as anomalies. The Gaussian Mixture Model (GMM), an unsupervised machine learning model, was employed to analyze these side-channel signals. The results demonstrate the effectiveness of the proposed detection technique in accurately identifying hardware Trojans.

Large Language Models for designing secure Integrated Circuits
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The increasing complexity of modern SoCs demands sophisticated verification methodologies, particularly in security-critical applications. Simultaneously, Large Language Models (LLMs) have demonstrated rapid advancements in various domains, offering novel capabilities in automation, reasoning, and pattern recognition. This research explores the application of LLMs in enhancing security-focused verification techniques, including fuzzing, assertion-based security property verification, information flow tracking, penetration testing, and concolic testing. By leveraging LLMs' adaptability and learning paradigms, we aim to optimize verification efficiency, improve threat detection, and strengthen overall chip security. In this presentation, we provide an overview of current security solutions that leverage LLMs, emphasizing their strengths and limitations. We assess how effectively they evaluate the security features of modern, complex SoCs and identify the challenges involved in deploying LLMs for large-scale industry designs.

Apple New Silicon Initiative
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Academic-industry partnerships rooted in enriching educational curricula can create talent pipelines and pathways to success for a broad spectrum of engineering students. These initiatives must include carefully designed elements that leverage the strengths of both industry and academia, facilitating impactful connections. The New Silicon Initiative (NSI) program, launched by Apple in 2019, and expanded to four HBCUs in 2021, was developed with this objective in mind, incorporating key components tailored to the needs of each partner university. The

partnership aims to foster educational excellence in Integrated Circuit (IC) design, computer architecture, and hardware engineering by connecting professionals in the field with faculty and students, promoting project-based learning, and advancing research. This talk will review the successes, challenges, and adaptations of the program and, critically, the learnings that have been unlocked for both the industry and universities.

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